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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,011	07/03/2002	Gilbert Wolrich	10559-312US1	5760

7590 07/27/2004

Dennis G Maloney
Fish & Richardson
225 Franklin Street
Boston, MA 02110-2804

EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,011	WOLRICH ET AL.	
	Examiner	Art Unit	
	William M. Treat	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-36 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-23, 26, and 30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al. (APRIL: A Processor Architecture for Multiprocessing).

4. Agarwal taught an instruction causing a reference to an address in a memory shared among threads executing in microprocessors while a context of the thread related to the instruction is interactive as in claims l and 30 (p. 104. last paragraph; p. l05, third paragraph; and pp. 1108-109, Section 4).

5. Agarwal taught appropriate editing and clearing of user-specified bits as in claims 2 and 31-32 (p. 109, table 2; and p. 110, 4th paragraph). Since Agarawal can set and clear user-specified bits for each word, he can inherently set multiple bits in a longword.

6. Agarwal taught an appropriate transfer register in a cache as in claims 3, 5, 9, and 35 (p. 1 10, Section 6.l). Note that the APRIL/ALEWIFE design is based on a RISC/SPARC processor which operates on data in the internal processor registers; therefore, the cache locations must represent interim transit registers prior to loading into the internal registers. Also, inherently, the instruction must contain sufficient data to tell the processor how to keep the data of each of the 4 possible threads in APRIL (p. l06, sixth paragraph) separated in both the cache and the registers.

7. Agarwal taught locking and unlocking memory based on the command to the extent claimed in claims 4, 6, and 34 (p. 106, 7th and 8th paragraphs and p. lo8, 3rd paragraph). The full/empty bits can effectively lock other instructions out as in an empty bit locking out an instruction seeking to read from a location. Also, since APRIL is designed primarily for a shared-memory multiprocessor with strongly coherent caches it must inherently prevent corruption of data by some form of lock to prevent the actions of one processor corrupting data while another processor is accessing it (p. 107, 6th paragraph).

8. As to claim 36, it fails to teach or define in any material way over rejected claims 34 and 35 (see paragraphs 6 and 7, *supra*).

9. As to claims 7-8, 10-12, 15-18, and 33, these are inherent capabilities of APRIL instructions based on its use of the SPARC processor instruction set 1 (pp. 109-110, Section 5) which contains such capabilities. Applicant has claimed individual instructions with individual capabilities and not one instruction with multiple capabilities based on its multiple fields.

10. As to claims 19-23 and 26, Agarwal's full/empty bits which are programmer determinable represent tokens which accomplish the appropriate actions (p. 108, 3rd paragraph).

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 24-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (APRIL: A Processor Architecture for Multiprocessing).

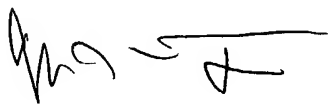
14. The examiner takes Official Notice of the fact that use of prioritized queues and ordered queues as in claims 24-25 to optimize access to processing cycles by threads most likely to be in an executable state is known in the art. Agarwal would be motivated to utilize such queue structures in his system because swapping in a blocked thread could cost hundreds of clock cycles thereby reducing his system's efficiency.

15. As to claims 27-29, these are merely conventional forms of memory. Agarwal has instructions to access memory. Using conventional forms of memory as the memory being accessed would save on cost of product over use of non-conventional memory and result in well-known, reliable designs for the memory.

16. Any inquiry concerning this communication should be directed to William M. Treat at telephone number 703 305 9699. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER